

NISIN

内嵌式触摸液晶显示模组规格承认书

(IN-CELL) LCM Specifications for Approval

客户： 客户型号：			NS350HD3005AZ01		
批准 APPROVED	审核 CHECKED	拟制 DESIGNED	批准 APPROVED	审核 CHECKED	拟制 DESIGNED



修改记录

日期	版本	修改内容	页数	拟制
2021-03-27	V00	初版发行	所有	

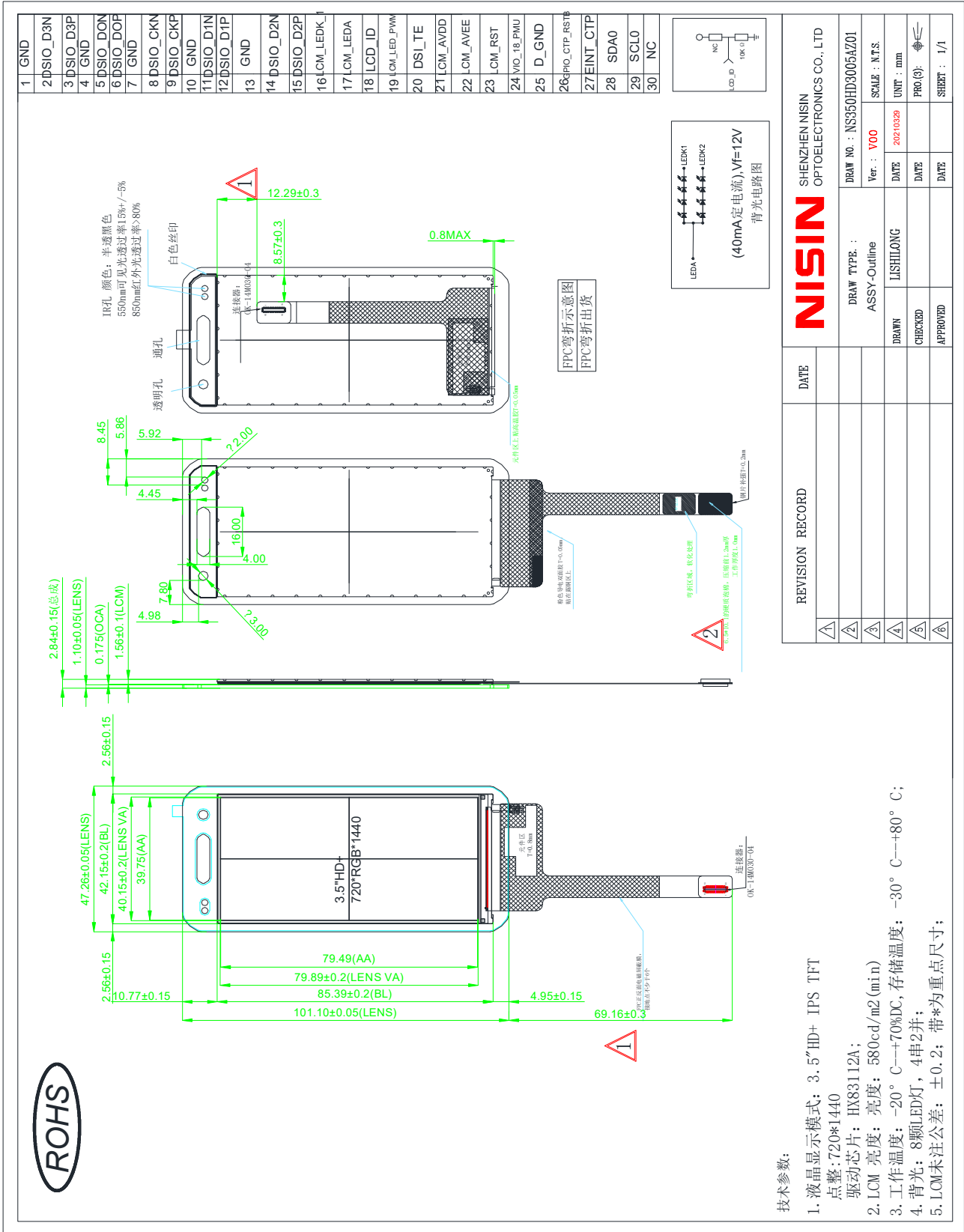
目录

1.产品规格 (Product Specifications)	4
2.产品图纸 (Product Drawings)	5
3.接口定义 (The Interface Definition)	6
4.电性特性 (Electrical Characteristics)	7
4.1 ABSOLUTE MAXIMUM RATINGS	7
4.2 DC CHARACTERISTICS	7
4.3 AC CHARACTERISTICS	8
4.4 MCU and Display Module Interface Conflagration	13
5. 显示初始化代码(Display Initial code)	14
6. 可靠性实验测试 (Reliability Test Conditions And Methods)	15
7. 光电参数 (Optical Characteristics)	16
7.1 光学规格 (Optical Specifications)	16
7.2 视角定义 (Description of View Angle)	17
8.检验标准 (Inspection standard)	18
8.1 Inspection conditions is as follows	18
8.2 LCD area definition	18
8.3 Routine inspection standards	19
9.模组使用注意事项 (Precautions for Use of LCD Modules)	21

1.产品规格 (Product Specifications)

面板类型 (Panel Type)	LTPS TFT
面板尺寸 (Panel Size)	3.5 inch
显示类型 (Display Type)	Normal Black
分辨率 (Resolution)	720(RGB) x 1440 (dot)
显示点间距 (Dot Pitch)	0.055mm X 0.055mm
显示色彩 (color)	16.7M
视角 (View Angle)	ALL
显示驱动 IC (Display Driver IC)	HX83112A
接口类型 (Interface Type)	MIPI 4 Lane
触摸类弄 (TP Type)	INCELL
触摸 IC (TP IC)	HX83112A
触摸接口类型 (TP Interface)	I2C
外形尺寸 (Dimensions)	47.26(H) X 101.10(V) X 2.84(T) (mm)
显示区尺寸 (Display area)	39.74x 74.49 (mm)
背光 (Back Light)	600 Cd/m ² (TYP)
触摸点数 Touch points	5
触摸按键 Touch Key Number	0

2. 产品图纸 (Product Drawings)



4.电性特性 (Electrical Characteristics)

4.1 ABSOLUTE MAXIMUM RATINGS

8.1 Absolute maximum ratings

The absolute maximum ratings are list on

- (1) VDD1, VSSD must be maintained.
- (2) To make sure $VDD1 \geq VSSD$.
- (3) To make sure $VSP \geq VSSA$.
- (4) To make sure $VSSA \geq VSN$.
- (5) To make sure $VGH \geq VSSA$.
- (6) To make sure $VSSA \geq VGL$, $VGH + |VGL| < 32V$.
- (7) To make sure $VGHO \geq VSSA$.
- (8) To make sure $VSSA \geq VGLO$.
- (9) For die and wafer products, specified up to +85°C.
- (10) This temperature specifications apply to the TCP package.
- (11) This specifications include input signals but without following: HS_CP, HS_CN, HS_D0P, HS_D0N, HS_D1P, HS_D1N, HS_D2P, HS_D2N, HS_D3P, HS_D3N.
- (12) This specifications include following signals: HS_CP, HS_CN, HS_D0P, HS_D0N, HS_D1P, HS_D1N, HS_D2P, HS_D2N, HS_D3P, HS_D3N.

Table 8.1 When used out of the absolute maximum ratings, the LSI may be permanently damaged. Using the LSI within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the LSI will malfunction and cause poor reliability.

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Power supply voltage 1 ⁽¹⁾⁽²⁾	VDD1 - VSSD	-0.3	-	+2.15	V
Power supply voltage 2 ⁽³⁾	VSP - VSSA	-0.3	-	+6.5	V
Power supply voltage 3 ⁽⁴⁾	VSSA - VSN	+0.2	-	-6.5	V
Power supply voltage 4 ⁽⁵⁾	VGH - VSSA	-0.3	-	+16	V
Power supply voltage 5 ⁽⁶⁾	VSSA - VGL	-15	-	+0.2	V
Power supply voltage 6 ⁽⁷⁾	VGHO - VSSA	-0.3	-	+15.6	V
Power supply voltage 7 ⁽⁸⁾	VSSA - VGLO	-13.6	-	+0.2	V
Power supply voltage 8	VDDD - VSSD	0	-	1.6	V
Operating temperature ⁽⁹⁾	T _A	-40	-	+85	°C
Storage temperature ⁽¹⁰⁾	T _{stg}	-55	-	+110	°C
Input voltage ⁽¹¹⁾	V _{in}	-0.3	-	VDD1+0.3	V
HS input voltage ⁽¹²⁾	V _{HSIN}	-0.3	-	+2	V

Note: (1) VDD1, VSSD must be maintained.

(2) To make sure $VDD1 \geq VSSD$.

(3) To make sure $VSP \geq VSSA$.

(4) To make sure $VSSA \geq VSN$.

(5) To make sure $VGH \geq VSSA$.

(6) To make sure $VSSA \geq VGL$, $VGH + |VGL| < 32V$.

(7) To make sure $VGHO \geq VSSA$.

(8) To make sure $VSSA \geq VGLO$.

(9) For die and wafer products, specified up to +85°C.

(10) This temperature specifications apply to the TCP package.

(11) This specifications include input signals but without following: HS_CP, HS_CN, HS_D0P, HS_D0N, HS_D1P, HS_D1N, HS_D2P, HS_D2N, HS_D3P, HS_D3N.

(12) This specifications include following signals: HS_CP, HS_CN, HS_D0P, HS_D0N, HS_D1P, HS_D1N, HS_D2P, HS_D2N, HS_D3P, HS_D3N.

4.2 DC CHARACTERISTICS

DATA SHEET Preliminary V00.11

8.2 DC characteristics (VDD1=1.8V, TA=25 °C)

Parameter	Symbol	Test condition	Spec.			Unit
			Min.	Typ.	Max.	
Input high voltage	V _{IH}	VDD1=1.65~1.95V	0.7 VDD1	-	VDD1	V
Input low voltage	V _{IL}		VSSD	-	0.3 VDD1	V
Output high voltage	V _{OH1}	I _{OH} =-1.0 mA	0.8 VDD1	-	-	V
Output low voltage	V _{OL1}	VDD1=1.65~1.95V I _{OL} =1.0 mA	VSSD	-	0.2 VDD1	V
Logic high level input current	I _{IH}	RESX, DCX, RDX, CSX, SCL_WRX, SDI_SDA	-	-	1	μA
Logic low level input current	I _{IL}	RESX, DCX, RDX, CSX, SCL_WRX, SDI_SDA	-1	-	-	μA
Current consumption SLP IN mode (VDD1-VSSD)	I _{ST(VDD1)}	VDD1=1.8V VSP=5.5V VSN=5.5V TA=25°C	-	-	3500	μA
Current consumption SLP IN mode (VSP-VSSA)	I _{ST(VSP)}		-	-	220	μA
Current consumption SLP IN mode (VSSA-VSN)	I _{ST(VSN)}		-	-	50	μA
Current consumption DSTB mode (VDD1-VSSD)	I _{DSTB(VDD1)}	VDD1=1.8V VSP=5.5V VSN=5.5V TA=25°C	-	-	80	μA
Current consumption DSTB mode (VSP-VSSA)	I _{DSTB(VSP)}		-	-	50	μA
Current consumption DSTB mode (VSSA-VSN)	I _{DSTB(VSN)}		-	-	50	μA
Oscillator tolerance ⁽¹⁾	ΔOSC	TA= -40°C ~ +85°C	-2	-	2	%

Note: (1) Oscillator tolerance with auto tracking.

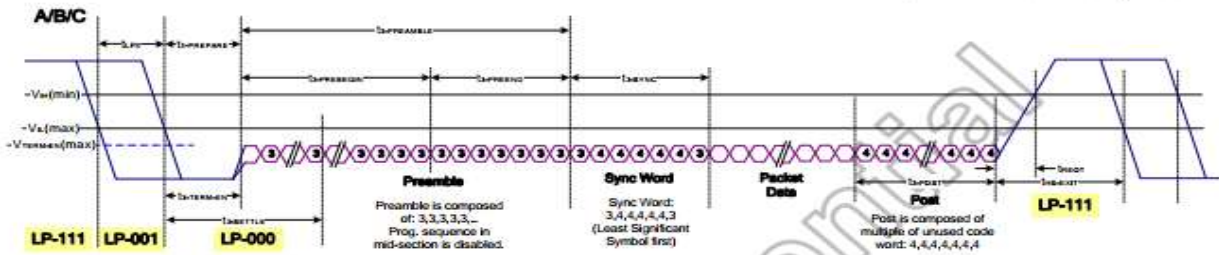
Table 8.2: DC characteristics

4.3 AC CHARACTERISTICS

4.3.1. MIPI Interface Characteristics

High Speed Mode – Clock Channel Timing

DATA SHEET Preliminary V00.11



Parameter	Description	Min	Typ	Max	Unit
t _{3-PREPARE}	Time that the transmitter drives the 3-wire LP-000 line state immediately before the HS_+x line state starting the HS transmission.	38	50	95	ns
t _{3-PREBEGIN}	Begins at the first differential state	140		448	UI
t _{3-PREEND}	The process for switching the lane in HS mode with '333333' before sync word '3444443'		7		UI
t _{3-POST}	The receiver identifies the end of packet data when it detects a sequence of '4444444' symbols.	168	224		UI

Figure 4.28: High speed data transmission timing sequence (C-Option)

4.2.2.5 High speed data transmission

The display module can enter High Speed Data Transmission when Clock Lane in the High Speed Clock Mode. All Data Lane enter High Speed Data Transmission synchronously but may end at different time. Data Lane enter High Speed Data Transmission flow: LP-11→LP-01→LP-00→SoT (0001_1101). And exit High Speed Data Transmission flow: Toggles differential state immediately after last payload data bit and keeps that state for a time $T_{HS-TRAIL}$.

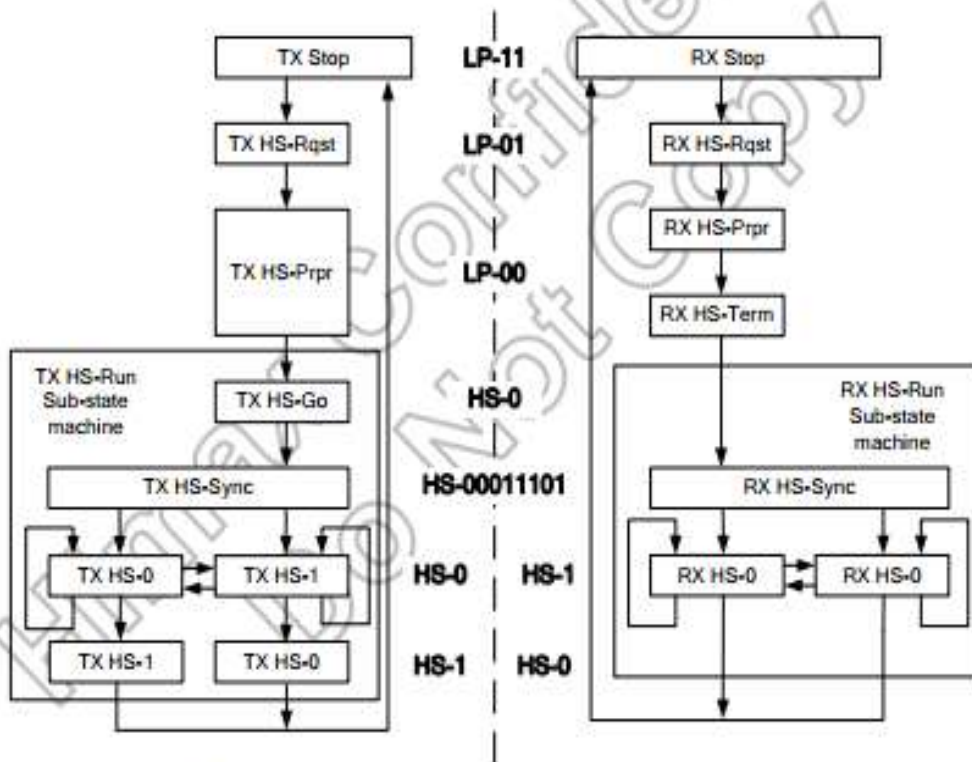


Figure 4.14: High speed data transmission state machine (D-Option)

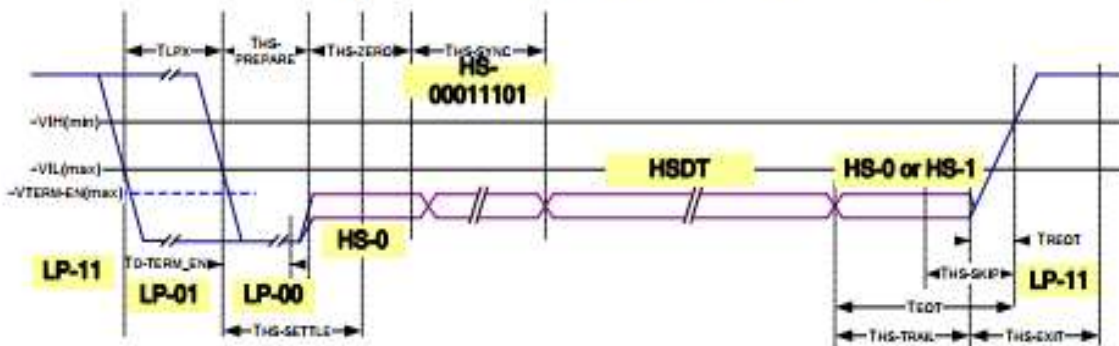


Figure 4.15: High speed data transmission timing sequence (D-Option)

4.3.2 复位时序 RESET Timing Characteristics

7.3.2 Reset Timing Characteristics

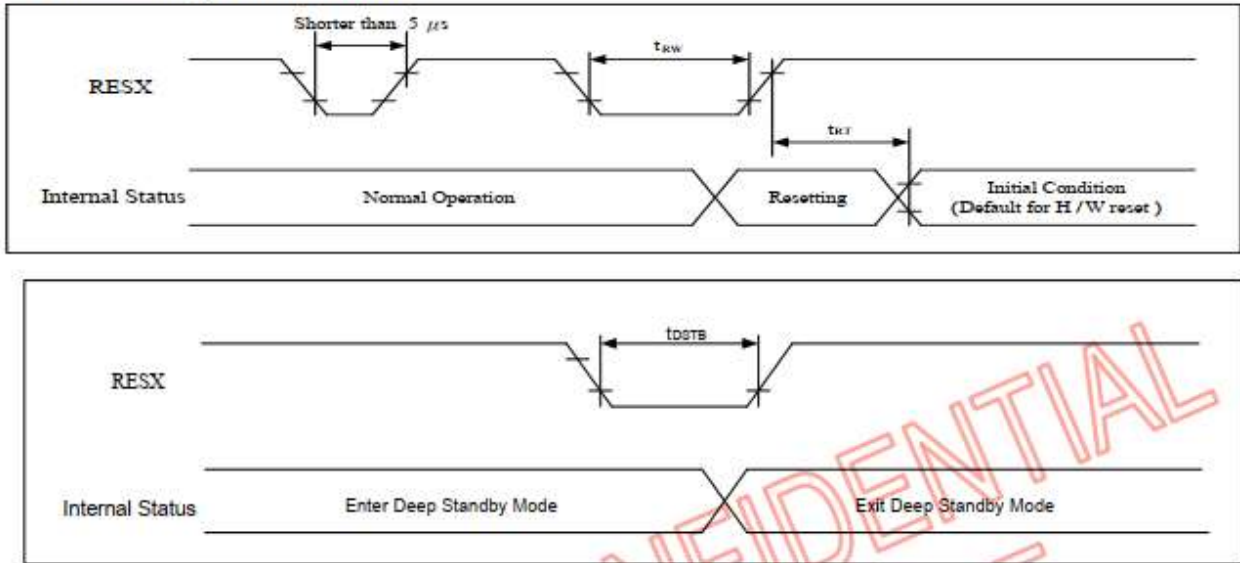


Figure 7.3.2 Reset Operation

Table 7.3.2 Reset Timing Characteristics VDDI=1.65~1.95V

Signal	Symbol	Parameter	Min.	Max.	Unit
RESX	t_{RW}	Reset pulse duration	10(Note)	-	us
	t_{RT}	Reset cancel	-	10(Note)	ms
			-	120(Note)	ms
	t_{DSTB}	Reset pulse duration	3	-	ms

Note :

- The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (t_{RT}) within 10 ms after a rising edge of RESX.
- Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below :
- During the Resetting period, the display will be blanked(The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts at Sleep-Out status. The display remains the blank state in Sleep-In mode). Then return to Default condition for Hardware Reset
- Spike Rejection also applies during a valid reset pulse as shown below :



- When RESET applied during Sleep-In Mode.
(RESET active during Sleep-in mode)
- When RESET applied during Sleep-Out Mode.
-It is necessary to wait 10ms after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 ms.

4.3.4 Power on / off Sequence

DATA SHEET Preliminary V00.11

5.12.1 VDD1/(VDDD)/VSP/VSN input power sequence

	Description	Min.	Typ.	Max.	Unit	Note
T1	VDD1/(VDDD) to VSP	1	2	-	ms	
T2	VSP to VSN	1	2	-	ms	
T3	VDD1 to MIPI Lane	1	2	-	ms	
T4	Power Ready to Global Reset	1	2	-	ms	
T5	Global Reset Keep Low	1	2	-	ms	TP Reset is the same.
T6	Global Reset to Sleep Out	25	48	-	ms	T9+T10+T11
T7	Sleep Out to Light On	60	83	-	ms	
T8	Touch Baseline Calibration	24	40	80	ms	
T9	Reset to Flash Reload	4	5	-	ms	
T10	Flash Reload time	20	40	-	ms	Default: 8MHz
T11	Display initial code by FW	1	3	5	ms	
T12	Sleep Out to Display On	1	10	T7-20	ms	
T13	Display On to IC Ready	20	T7-T12	-	ms	
T14	Last cmd to Backlight On	30	-	-	ms	

Table 5.8: Time description of normally power on sequence - with flash.

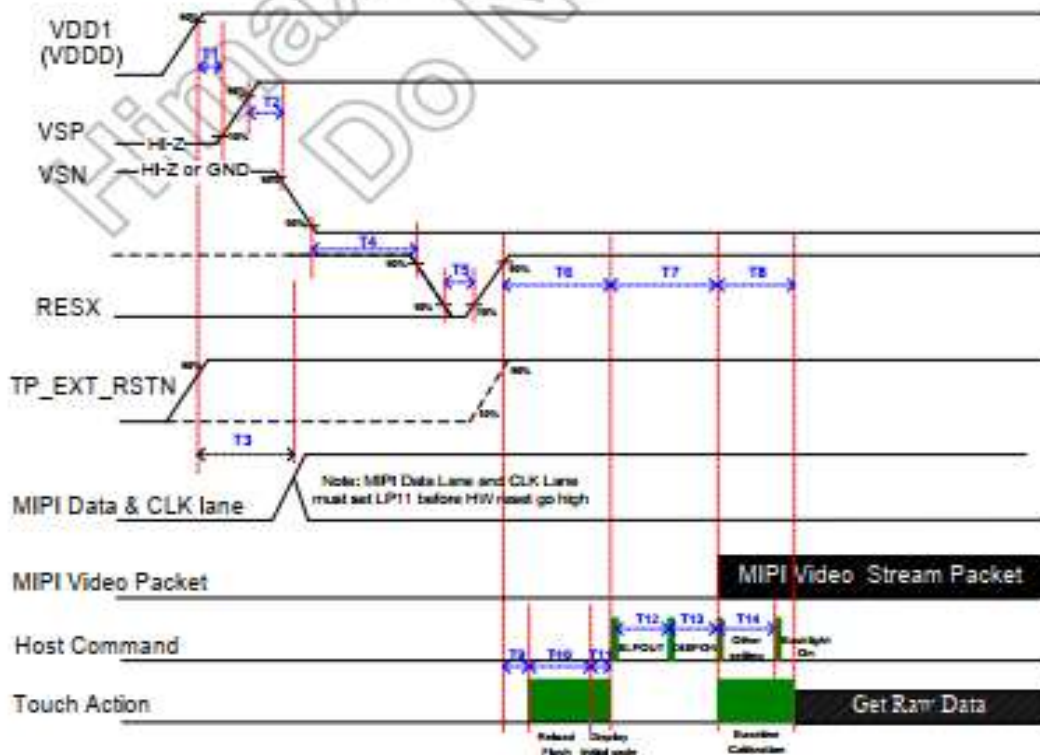


Figure 5.22: VDD1/(VDDD)/VSP/VSN input power on sequence - with flash

5. 显示初始化代码 (Display Initial code)

Width 720

Height 1440

VS_sync 5

VS_BP 5

VS_FP 50

HS_sync 44 //8

HS_BP 40//12

HS_FP 40//48

//Set_EXTC

Payload[B9 83 11 2A]

//Set_CF

Payload[CF 00 14 00 C0]

//Set_PANEL

PacketHeader[15 CC 08]

//Set_CABC

Payload[C9 04 0A 8C 01]

//Set_power

Payload[B1 08 2F 2F 80 80 4A 4F AA]

//Set_display

Payload[B2 00 02 00 52 A0 00 08 30 31 11 15 00 10 A3 87]

//Set_D2

Payload[D2 32 32]

//Set_cycles

Payload[B4 0B E1 0B E1 0B E1 0B E1 0B E1 0B E1 00 FF 00 FF 00 00 0C 0F 00 3A 08 0D 0F 00 3A]

//Set_C7

Payload[C7 00 00 04 E0 33 00 20 40]

//Set_Vcom

Payload[B6 7B 7B E3]

//Set_GIP_0

Payload[D3 C0 00 00 00 00 01 00 0A 0A 09 09 00 0F 0B 0B 0B 0B 32 10 09 00 09 32 10 0F 00 0F 32 10 00 00 00 00 00 00 00 00 0A 05 AB]

Delay 5ms

//Set_BANK

PacketHeader[15 BD 01]

//Set_CB

Payload[CB 25 11 01]

//Set_BANK

PacketHeader[15 BD 00]

//Set_GIP_Fmapping

Payload[D5 18 30 19 18 20 40 18 18 30 20 31 19 2F 01 40 2F 18 31 18 03 18 05 00 07 02 09 04 18 06 18 08 18 18 18 18]

Delay 5ms

//Set_GIP_Bmapping

NISIN

```
Payload[D6 18 18 18 18 18 18 18 18 18 18 18 18 18 18 18 18 30 19 18 20 40 18 18 30 20 31 19 2F 08 40 2F 18 31 18 06 18 04 09 02 07 00 05 18 03 18 01 18 18 18 18]
Delay 5ms
//Set_D8
Payload[D8 AA AA AA FA FF AA AA AB AA AA BF FA AA AA EA AA AA AB AA AA AA]
//Set_BANK
PacketHeader[15 BD 01 ]
//Set_D81
Payload[D8 AA AB BA BF FF AA AA AA AF FA BF FA AA AB BA BF FF AA AA AA AF FA BF FA]
//Set_BANK
PacketHeader[15 BD 02 ]
//Set_D82
Payload[D8 AA AB BA BF FF AA AA AA AF FA BF FA]
//Set_BANK
PacketHeader[15 BD 03 ]
//Set_D83
Payload[D8 AA AA AA EA AA AA AA AB AA AA AA AA AA AB BA BF FF AA AA AA AF FA BF FA]
//Set_BANK
PacketHeader[15 BD 00 ]
//Set_E7
PacketHeader[39 18 00 XX]
Payload[E7 0F 0F 1E 82 1E 82 00 50 02 02 00 00 02 02 02 05 14 14 32 B9 23 B9 08]
//Set_BANK
PacketHeader[15 BD 01 ]
//Set_E71
Payload[E7 02 00 5A 01 64 0E 3C 0F]
//Set_BANK
PacketHeader[15 BD 02 ]
//Set_E72
PacketHeader[39 1E 00 XX]
Payload[E7 00 00 08 00 01 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 04 00 00 00 00 02 00]
//Set_BANK
PacketHeader[15 BD 00 ]
//Set_E9
PacketHeader[15 E9 C3 ]
//Set_CB1
Payload[CB D2 63]
//Set_E9
PacketHeader[15 E9 3F ]
//Set_DGCLUT
PacketHeader[15 C1 01 ]
//Set_BANK
PacketHeader[15 BD 01 ]
```

```
//Set_E9
PacketHeader[15 E9 C8 ]
//Set_GIP_01
PacketHeader[15 D3 81 ]
Delay 5ms
//Set_E9
PacketHeader[15 E9 3F ]
//Set_BANK
PacketHeader[15 BD 00 ]
//Set_DGCLUT
Payload[C1 01 00]
//Set_BANK
PacketHeader[15 BD 01 ]
//Set_DGCLUT1
Payload[C1 FF FA F5 EF EB E6 E1 D7 D2 CD C7 C2 BE B8 B3 AE A9 A3 9E 95 8C 83 7B 73 6B 63 5B 54 4D 47 40 3A 33 2D 26 20 1A 14 0E 09 06 04
02 01 00 03 56 AF 24 3D 14 0E 1D 5A B8 3A 40]
//Set_BANK
PacketHeader[15 BD 02 ]
//Set_DGCLUT2
Payload[C1 FF FA F5 EF EB E6 E1 D7 D2 CD C7 C2 BE B8 B3 AE A9 A3 9E 95 8C 83 7B 73 6B 63 5B 54 4D 47 40 3A 33 2D 26 20 1A 14 0E 09 06 04
02 01 00 03 56 AF 24 3D 14 0E 1D 5A B8 3A 40]
//Set_BANK
PacketHeader[15 BD 03 ]
//Set_DGCLUT3
Payload[C1 FF FA F5 EF EB E6 E1 D7 D2 CD C7 C2 BE B8 B3 AE A9 A3 9E 95 8C 83 7B 73 6B 63 5B 54 4D 47 40 3A 33 2D 26 20 1A 14 0E 09 06 04
02 01 00 03 56 AF 24 3D 14 0E 1D 5A B8 3A 40]
//Set_BANK
PacketHeader[15 BD 00 ]
//Sleep_out
PacketHeader[05 11 00]
Delay 120ms
//Display_on
PacketHeader[05 29 00]
Delay 10ms
```

6.可靠性实验测试(Reliability Test Conditions And Methods)

序号	试验项目	试验条件及方法	试验设备	检验项目	检验工具
1	高温高湿(静、动态)试验	温度 $60^{\circ}\text{C} \pm 3^{\circ}\text{C}$, 湿度 $90\% \pm 3\%$, 要求选择时间分别为 96 小时, 静、动态(产品点亮)在室温下恢复 2 小时后进行外观, 显示功能检查。	恒温恒湿试验机	检验外观、功能、抗腐蚀性	目视/测试架/客户样机/显微镜
2	高、低温冲击试验	静态 -30°C (30 分钟) \sim 80°C (30 分钟) \sim -30°C (30 分钟), 24 个循环, 在室温下恢复 2 小时后进行外观, 显示功能检查。	冷热冲击试验机	检验外观、功能	
3	高温存贮试验	常温 $60^{\circ}\text{C} + 3^{\circ}\text{C}$ 、宽温 $70^{\circ}\text{C} + / - 3^{\circ}\text{C}$ 、96 小时后在室温状态下恢复 1 小时在 2 小时内完成外观、显示功能检查。	烤箱	检验外观、功能	目视/测试架/客户样机
5	低温存贮试验	4.1 常温 $-20^{\circ}\text{C} + / - 3^{\circ}\text{C}$ 、宽温 $-30^{\circ}\text{C} + / - 3^{\circ}\text{C}$ 、条件的试验箱内保存 96 小时后在室温状态下恢复 1 小时, 在 2 小时完成外观、显示功能检查, 特别注意检查是否有漏液、断线、腐蚀、偏光片不良现象。	低温冰箱	检验外观、功能	
5	包装模组跌落试验	跌落高度为 60CM, 正反面各 2 次, 带 T/P 跌落高度为 80CM, 正反面各 2 次	包装模组跌落架	测试电性能无异常、外观检验无破损, 无脱离现象	目视/测试架/客户样机
6	盐雾试验	1. 标准条件: 中性盐雾试验 (NSS 试验): 5% 的氯化钠盐水溶液, 溶液 PH 值中性(6~7), 试验温度 $35 \pm 2^{\circ}\text{C}$, 盐雾的沉降率在 $1 \sim 2\text{ml}/80\text{cm}^2 \cdot \text{h}$ 之间, 时间 24h。2. 其它特殊要求条件: 醋酸盐雾试验 (ASS 试验): 5% 氯化钠溶液中配入冰醋酸, 溶液 PH 值为 3 左右, 试验温度 $35 \pm 2^{\circ}\text{C}$, 盐雾的沉降率在 $1 \sim 2\text{ml}/80\text{cm}^2 \cdot \text{h}$ 之间, 时间 24h。	盐雾试验设备	检验外观、功能, 盐雾试验结果的判定方法, 腐蚀物出现判定方法: 定性判定, 试验后功能测试应 OK, 外观观察产品无腐蚀现象产生。	目视/测试架/客户样机/显微镜
7	ESD 防静电试验	测试架测试状态下试验: 接触 4KV, 非接触(空气) 8KV 放电测试	防静电枪(尖头接触放电, 圆头空气放电)	检验外观、功能	目视/测试架

7. 光电参数 (Optical Characteristics)

7.1 光学规格 (Optical Specifications)

HTA7704B
6. OPTICAL SPECIFICATION

Item	Symbol	Condition	Specification			Unit	Remark	Notes
			Min.	Typ.	Max.			
T% (w/o APCF, w/o haze) @ C-light	T%	1.Viewing normal angle $\theta_x=\theta_y=0^\circ$ (Center) 2.At 25°C	3.01%	3.49%	--	%	Center	All left side data are based on INX's following condition (at 25 °C) 1. LC : AAS 2.BLU : C-Light 3. Polarizer: CVT1764KDUHC3 4.Machine : DMS 900 5.V LC : Vbright \geq 5.4V Vdark \leq 0.2V
Contrast Ratio (w/o WPA)	CR		1000	1500	--	--	Center Note (1)	
Response Time (w/o WPA)	Ton+Toff		--	--	30	ms	Center Note (2)	
Viewing Angle	Hor.	θ_{x+}	80	--	--	deg	Note (3)	
		θ_{x-}	80	--	--			
	Ver.	θ_{y+}	80	--	--			
		θ_{y-}	80	--	--			
CF only Chromaticity (CIE1931)	Red	Rx	0.641	0.661	0.681	--	--	
		Ry	0.301	0.321	0.341	--	--	
	Green	Gx	0.244	0.264	0.284	--	--	
		Gy	0.554	0.574	0.594	--	--	
	Blue	Bx	0.118	0.138	0.158	--	--	
		By	0.089	0.089	0.109	--	--	
	White	Wx	0.276	0.296	0.316	--	--	
		Wy	0.301	0.321	0.341	--	--	
	NTSC	xy	65.9	70.9	--	%	--	

*Note (1) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

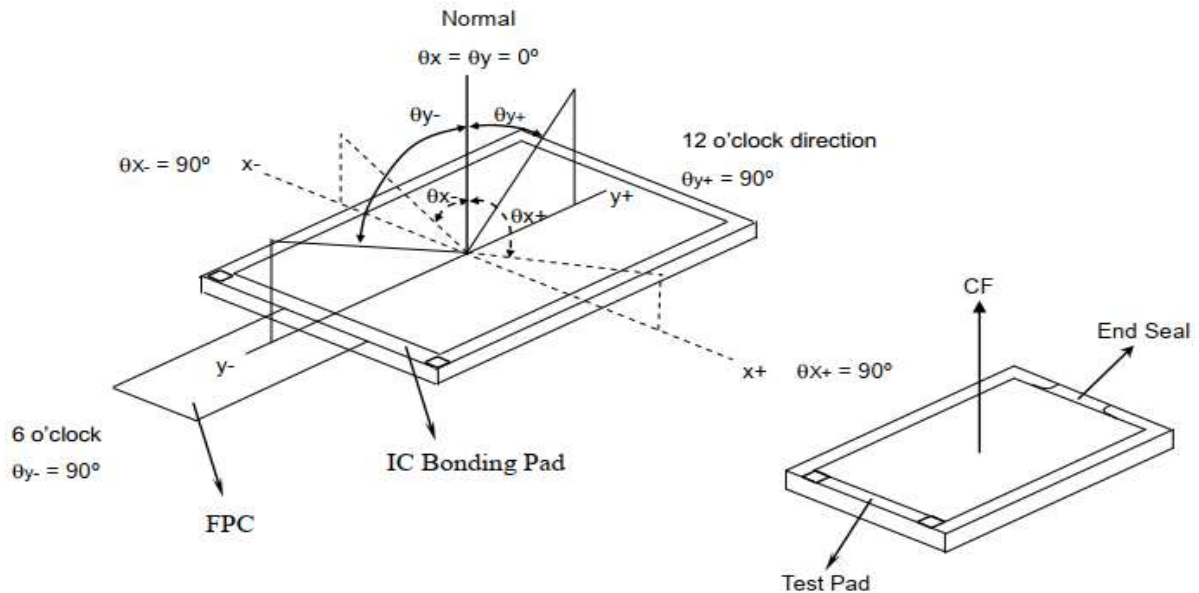
$$\text{Contrast Ratio (CR)} = L_{255} / L_0$$

L 255 : Luminance of gray level 255

L 0: Luminance of gray level 0

7.2 视角定义 (Description of View Angle)

*Note(3) Definition of Viewing Angle



8. 检验标准 (Inspection standard)

8.1 Inspection conditions is as follows

- 1) Viewing angle is within $\pm 30^\circ$ from vertical direction, as fig 1
- 2) Viewing angle is the angle defined in the drawing
- 3) Ambient temperature is approximately $25 \pm 5^\circ \text{C}$
- 4) Ambient luminance is about 300~500 Lux.

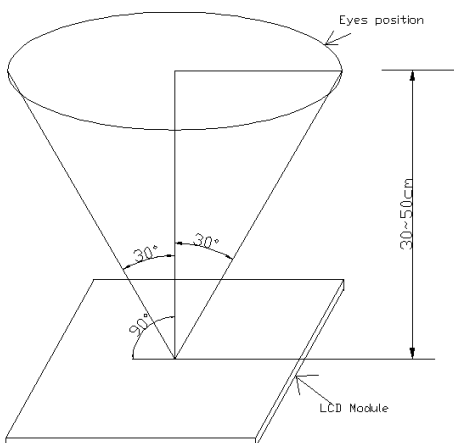
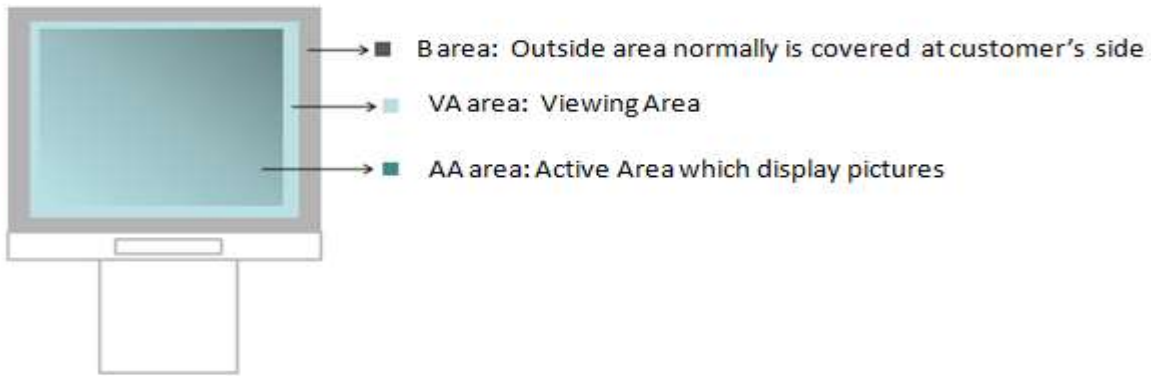
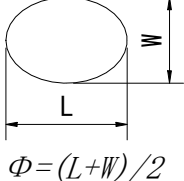


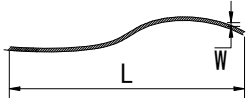
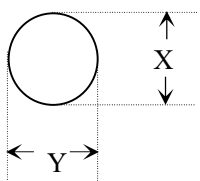
fig1

8.2 Panel area definition



8.3 Routine inspection standards

项目	不良定义	不良现象	判定标准		检验方法	
11.3.1	外观尺寸	与图纸尺寸不相符	NG		卡尺	
11.3.2	功能	显示少线	NG		目视	
		无显示	NG		目视	
		显示异常	NG		目视	主
		TP 功能不良, 无触摸	NG		目视/用手触摸	主
11.3.3	点亮产品可见及在LCD或T/P上有擦拭不掉的点状物	偏光片刺伤、脏点、圆形物、黑点 	LCM/总成 0.95 寸—2.4 寸		目视 (用菲淋卡比对)	次
			$\Phi \leq 0.10mm$	1、距产品30mm 目视不见忽略。 2、5mm 间距内只允许3个点。 3、显示区只允许10个点, 超过以上第2第3项则NG。		
			$0.10mm < \Phi \leq 0.15mm$	1		
			$\Phi > 0.15mm$	NG		
			0.15mm < Φ ≤ 0.2mm 按照 A-品入库			
			LCM/总成 > 2.4 寸—6.0 寸		$\Phi \leq 0.10mm$	

				2、显示区只允许 10 个点，超过以上任意一项则 NG			
			$0.1\text{mm} < \Phi \leq 0.15\text{mm}$	4 (TP、屏各允许 2 个)			
			$0.15\text{mm} < \Phi \leq 0.2\text{mm}$	2 (TP、屏各允许 1 个)			
			$\Phi > 0.2\text{mm}$	NG			
11.3.4	点亮产品可见及在 LCD 或 T/P 上有擦拭不掉的线状物/刮伤		LCM/总成 0.95 寸——6.0 寸		目视(用菲淋卡比对)	次	
			长(L)	宽(W)			允许个数
			$\leq 1\text{mm}$	$\leq 0.03\text{mm}$			2
			$\leq 2\text{mm}$	$0.03 < W \leq 0.05\text{mm}$			1
			$> 2\text{mm}$	$> 0.05\text{mm}$			NG
			两条线毛之间必须距离 5mm 以上 (0.95 寸—3.0 寸). 两条线毛之间必须距离 10mm 以上 (3.1 寸—6.0 寸).				
11.3.5	偏光片气泡	$\Phi = (X+Y) / 2$ 	尺寸	允许个数	在日光台灯下撕起保护膜, 距待测物 30cm 目视	次	
			1、 $\Phi \leq 0.1\text{mm}$ 2、不超过边框 1/3	不计 (密集不可)			
			$0.10 < \Phi \leq 0.2\text{mm}$	1			
			$\Phi > 0.2\text{mm}$	NG			
			$0.2 < \Phi \leq 1.5\text{mm}$, (边框以外)	3			
			0.95 寸-2.4 寸气泡间距大于 5mm 以上 >2.4 寸-6.0 寸气泡间距大于 10mm 以上				
11.3.6	T/P 及偏光片凹凸点	T/P: LCD 偏光片上有凹凸点	可视区有水纹 (擦拭不掉) 拒收 未进入可视区允收, 客户装机后不见允收		在同一视角下用样品比对	次	
11.3.7	Mura	边框四周或任一侧的色差、较画面深、区域云状不均、固定位置之图形凹	1.判定画面为 128 灰阶画面, 用 ND filter 盖住 mura 位置进行判定。		ND filter, 128 灰阶画面	次	

		陷状、封口部分较画面深的半圆形、一圈圈均匀的色差、线状 mura、黑画面可见因 spacer 聚集产生的 mura、均匀的实斜线、区域性斜线、Driver IC 与 TFT 匹配问题等原因的 mura	2、ND1.3 (ND5%可遮盖不见) 3、双方若有签 限度样品, 优先限度样品。		
--	--	--	--	--	--

9.模组使用注意事项 (Precautions for Use of LCD Modules)

- 12.1 如果接口定义内有定义 IM0, 请根据规格书 (4.接口定义) 内的定义做正确选择以匹配数据线的位数。
- 12.2 客户在做结构设计时, 请保证机壳开窗尺寸比触摸屏 V.A 单边少 0.3mm。泡棉开窗尺寸比触摸屏 V.A 单边大 0.2mm。
- 12.3 模组的主要部件 LCD 和 TP 都是由玻璃组成, 在测试、使用、移动过程中, 请轻拿轻放。当产品不带触摸屏时, 靠近 FPC 的屏幕两端绝对不能受力, 否则会导致玻璃破损和显示不良的发生。
- 12.4 粘合偏光片、背光、触摸屏的胶材是有机物质, 在接触到甲苯、乙醇、丙酮时, 会破坏粘性。在使用中, 请防止这些物质接触到产品。
- 12.5 如果显示表面掉落有灰尘、异物, 切忌用手直接擦拭。请用棉签轻轻挑擦。
- 12.6 如果 LCD 破损导致液晶泄露, 请不要让皮肤或衣服沾到液晶。如果不小心碰到, 请立即用肥皂和清水清洗。
- 12.7 用手直接接触显示区域会造成偏光片的损坏, 同时容易引起静电问题。
- 12.8 当模组运行时, 在显示区域施加压力会导致显示不正常。撤去外力, 重新开机, 可以恢复。
- 12.9 潮湿的环境可能引起玻璃 ITO 的腐蚀, 在使用中, 请确保湿度在 50%一下。